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An EMTP System Level Model of the PMAD DC Test Bed

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ABSTRACT

A *Power Management and Distribution Direct Current (PMAD DC)* test bed has been set up at the NASA Lewis Research Center to investigate *Space Station Freedom Electric Power System* issues. Efficiency of test bed operation significantly improves with a computer simulation model of the test bed as an adjunct tool of investigation. Such a model is developed using the *Electromagnetic Transients Program (EMTP)* and is available to the test bed developers and experimenters. The computer model is assembled on a modular basis. Device models of different types can be incorporated into the system model with only a few lines of code. A library of the various model types is created for this purpose. Simulation results and corresponding test bed results are presented to demonstrate model validity.

INTRODUCTION

NASA Lewis Research Center has the responsibility to oversee the design, fabrication, and assembly of the *Electric Power System (EPS)* for the *Space Station Freedom (SSF)*. From the early concepts to the present baseline, the EPS design has undergone many changes. One of the early concepts was to use a *20 kHz based ac distribution system*. Due to the immaturity of information about 20 kHz distribution, a test bed was set up to help collect the same. Since then, the test bed has kept in step with the evolving EPS, culminating in the present PMAD DC test bed for the *all dc EPS design*. [1].

Purpose of the Test Bed

The main purpose of the test bed is to evaluate system design concepts and issues, e.g., source system stability, fault protection system coordination, power quality, power control, etc.. The information gained from the test bed can be used by the prime contractor to facilitate overall development. Therefore, the test bed should be a sufficient representation of the EPS but it need not be an exact replica.

Purpose of the Test Bed Computer Model

The main purpose of the test bed computer model is to provide an environment where a proposed test bed run can be simulated to asses safe operating regions. In that respect it becomes very useful to the test bed operator. The computer model is also a useful tool for other investigations which can not be performed on the test bed due to time and cost constraints, e.g., parametric studies, evaluation of anomalous behavior, hardware operation at its design limits, evaluation of reconfiguration options, etc..

History of Test Bed Modeling

Test bed modeling efforts at Lewis began with the 20 kHz test bed. EASY5 was used as the modeling tool [2,3]. While an excellent tool for control system analysis and design, EASY5 is not well suited to model electrical distribution networks with attendant stiff systems. EMTP can model such networks very efficiently and is used as such, worldwide, by the utility industry. Recently, power electronic devices were successfully modeled on EMTP with help from its *Transient Analysis of Control Systems (TACS)* feature [4]. Such devices, while slowly populating the terrestrial power systems, are the basic components for the EPS. Initial EMTP models were based on circuit representation of the devices. Although faster to execute compared to EASY5 models, these were not fast enough to become building blocks for an end-to-end system level model. This led to the development of *functional models*, which simulate the input/output behavior of a device. The functional models achieved the necessary speed of execution for an end-to-end representation while

retaining sufficient fidelity to produce accurate system simulation results [5,6].

TEST BED CONFIGURATION AND DESCRIPTION

A test bed should include all the significant elements of the proposed EPS, both in types of hardware as well as the connecting elements of the system.

The PMAD DC test bed is equipped with the necessary hardware and software to study issues concerning the operation and control of the EPS [7,8]. Presently, it consists of one channel (Channel A) of *supporting development hardware*. This hardware is functionally equivalent to the hardware that will be used on the SSF but more readily available. Channel B will consist of *early breadboard versions of flight hardware*. Each channel contains the following hardware elements: 1) a solar array/simulator source, 2) a sequential shunt switching unit (SSU) to match the source output to the load, 3) a battery charge/discharge converter (BCDU) to regulate the battery source, 4) a dc-to-dc voltage converter (DDCU) to connect the 160V primary system to the 120V secondary system, 5) dc-to-dc load converters (LCU) for connecting the low voltage tertiary system (loads) to the secondary system, and 6) switchgear, both the regular and current limiting type, connecting different parts of the distribution network. Each hardware piece is protected against electrical faults and has the necessary controls for safe operation. Also, there are appropriate control and protection schemes for each channel. Although the channels can be operated independently of each other, cross-tying them near the source end is under consideration for evaluation of increased power channel size. Further details about the test bed layout, operation, protection and control system may be found in reference [7].

DESCRIPTIONS OF MODELS

The models have already been extensively described in reference [5]. Circuit level models were developed first to determine how they compared with those in EASY5, both for fidelity and execution time. Not all of the components were modeled at circuit level. While the circuit level models could be constructed from design information, the functional models required some form of hardware test data to determine their functionality.

Circuit Level Component Models

A typical hardware component has electric circuits in the power, control, and protection areas. Figure 1 shows the power processing component for a DDCU. It is inappropriate to model the control and protection schemes as circuits because it requires a very small integration time step size to correctly simulate such circuits. Since the same time step will be used for the entire simulation, it will result in very lengthy execution time. On the other hand, TACS can model such circuits functionally without requiring small integration time steps. Thus, only the power stage of the hardware was modeled at circuit level while the electronic circuitry in the control and protection system was modeled as functional equivalents in terms of digital logic and transfer function models using TACS. Electronic switches were represented as either ideal or diode switches. Filters were modeled as actual circuits. A pulse width modulation (PWM) device controls the switches in the power stage, typically operating at 40 kHz. This limits the choice of integration time step size to less than a few microseconds, resulting in lengthy execution times. Nevertheless, these models are useful in studies where, for example, voltage stress across the solid state switch is of concern.

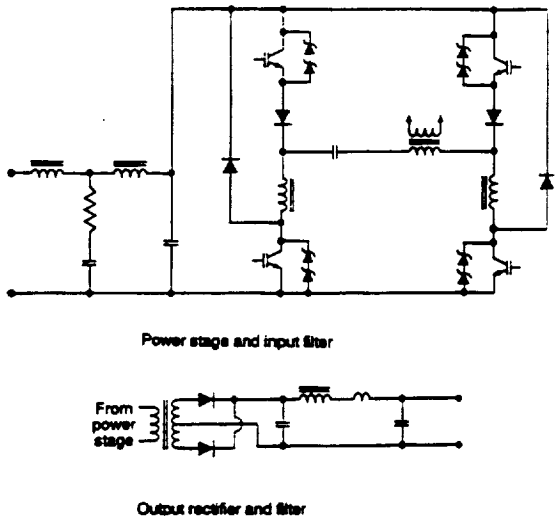

Fig. 1 Power Stage Circuit of a DDCU

Functional Component Models

It is clear from the previous discussion that system level simulation of the test bed involving many hardware pieces is not practical with circuit level component models. Functional models were developed as a compromise between fidelity and the ability to represent an end-to-end system using reasonable amount of computer resources. The performance of these models was validated against test results, examples of which are shown later in this paper. The main difference between the functional and the circuit level models is in the power stage modeling. The switches and the attendant PWM devices were eliminated, permitting a much larger integration time step size. Input/output relationships were now established using a controlled current source and a corresponding dependent voltage source. Complexity in the circuit level simulation of a DDCU is shown by figure 1. Figure 2 shows the functional model of the same DDCU.

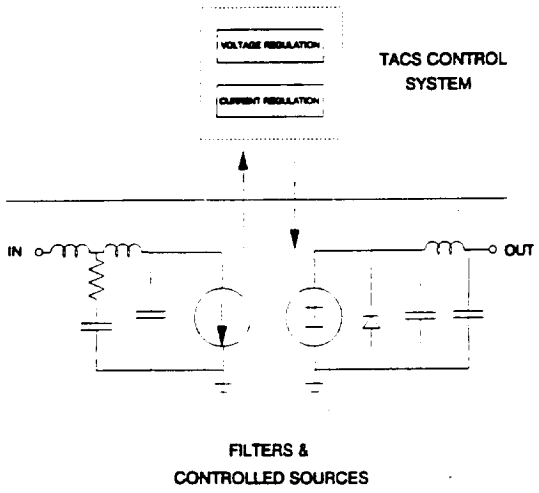

Fig. 2 Functional DDCU Model in EMTP

One of the main advantages of the functional models is the ability to use larger values of integration time steps permitting execution of end-to-end system simulation in a reasonable length of time. This entails some loss of fidelity, especially for the response of the input and output filters which were simulated as electric circuits. This does not, however, mean any numerical instability because of the inherent *stability of the implicit integration technique using* **trapezoidal rule** that EMTP employs [9].

Protection and Control System Models

Test bed protection system protects the individual pieces of hardware and brings the test bed to a safe state of operation upon the occurrence of an abnormality, e.g., a fault (short circuit), malfunction of a hardware, etc. [10]. Traditional protection schemes such as *over current and differential zone* are being implemented in the system level model. Any protection or control scheme that takes more than one second to complete its action will not be implemented in a transient, system level model of the test bed. Controls for maintaining hardware power quality have been implemented in the respective models. Control schemes such as load tripping based on under voltage condition will be implemented later.

System Model Configuration

The system model layout has the description of the electrical network and also has the information needed to execute a particular test case. Component modules are incorporated from a data base specifically created for that purpose.

The circuit level and the functional models are not intended to be mutually exclusive. A circuit level model could be connected into an otherwise entirely functional model environment for a specific purpose such as to test a circuit level model in the total system. Of course, the whole simulation will have to be run at the smaller time step as dictated by the circuit level model. This will not result in much higher execution time because the remaining, less complex functional models run much faster, even with small time steps, compared to a complex circuit level model. For this and other reasons the system model configuration was designed on a modular basis enabling replacement of component models with only a few lines of code.

MODEL VALIDATION

One of the functions of the test bed model is to predict operating conditions for the test bed. The model should behave similar to the actual test bed to have reasonable confidence in the simulation results. No model is an exact replica of the hardware it represents. It is more so with the functional models. Therefore, the models needed some fine tuning to match the test results (validation). Validation should take place, using the functional models, at the three levels of *test bed check out process,* namely at, component, subsystem, and system levels. Some examples of validation follow where only functional models of components were utilized.

Functional Component Model Validation

All of the test bed components are individually tested for correct input/output behavior. These tests provide data for functional component model validation.

A DDCU is subjected to a step load change, from a light to a heavy load condition. DDCU output current and voltage wave forms from the test are compared with simulation results and are shown in figures 3 and 4 respectively. The voltage feedback control loop gain in the model is adjusted to obtain the best possible match between the test data and simulation results. Figure 4 shows some mismatch between the respective DDCU output voltage plots. Because of the utilization of implicit integration, it is possible to reduce this mismatch by using a smaller integration time step and by plotting every data point. However, that will defeat the purpose of developing the functional models which were meant to be used for long term investigations (of the order of 1 sec) with large time steps (0.1 msec). The functional models behave properly within the limitations imposed upon them.

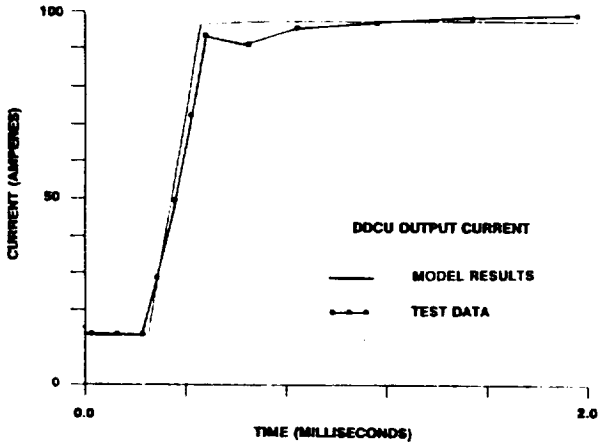

Fig. 3 Functional DDCU Model Validation Output Current — Step Load

Subsystem Level Validation

The test bed can be considered as a coherent connection of subsystems, each able to function somewhat independently. Thus, testing of subsystems in the test bed, before the final end-to-end integration, was a necessary step in the scheme of comprehensive testing. Data from one such test were used to validate the computer model. The primary source subsystem was tested to study the response of the solar array/simulator and SSU to step load changes. Initially the source subsystem is heavily loaded by connecting loads at both the main Bus Switching Unit (MBSU) and the Direct Current Switching Unit (DCSU). The load at DCSU is switched off to create the transient. Computer simulation for the test configuration was performed and results compared with test data as shown in figure 5. During this comparison the value of the voltage feedback control loop gain of the SSU was adjusted to obtain best possible match between test data and simulation results. Once again, the simulation results appear to be more damped compared to the test data. The reason for this was explained previously under functional component model validation.

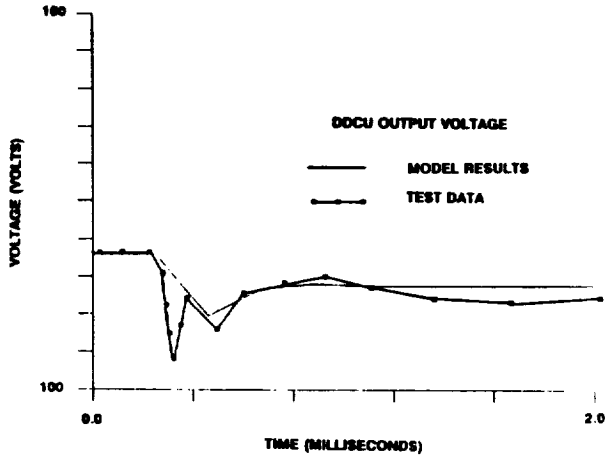

Fig. 4 Functional DDCU Model Validation Output Voltage — Step Load

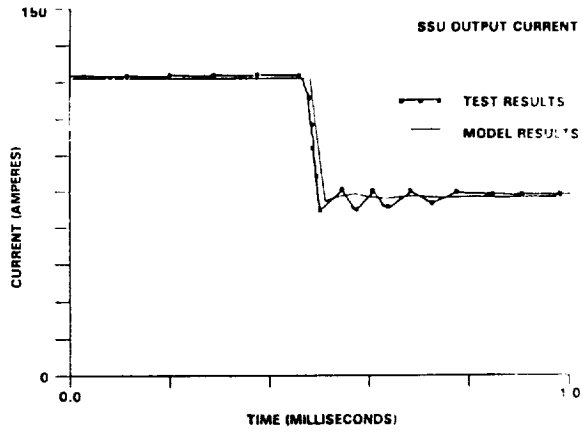

Fig. 5 Functional SSU Model Validation Output Current — Step Load

SIMULATION STUDY RESULTS

After the test bed model has been validated to a reasonable degree, it is ready to be used as a precursor for a test bed study or to be used for testing other possible operating scenarios which may or may not be repeated on the test bed. Figure 6 shows the block diagram of the present EMTP test bed layout. Two sample cases were run using this model. Results are presented and described.

Case Study No. 1

The start up process of the test bed consists of a series of events. The nature of the start up and shut down characteristics of the various hardware pieces of the EPS is of great concern, mainly because of the limited current capacity of the sources. Inrush currents caused by charging of input filters may affect the protection system operation.

Figure 7 shows the SSU output voltage and current when the 600 uF SSU and the 4000 uF DCSU bus capacitors are charging up in an unloaded system. The oscillatory nature of the current wave form is due to the R-L-C circuit formed by the bus capacitors being charged and cables connecting them.

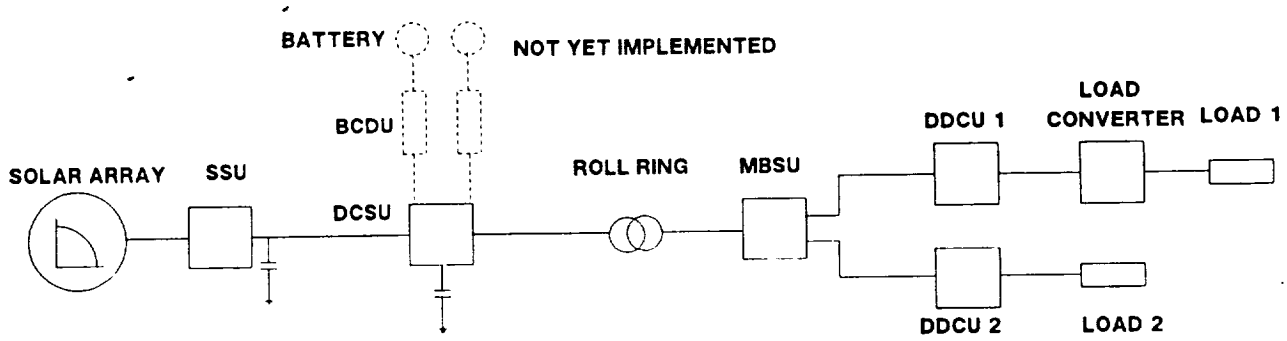

Fig. 6 EMTP Test Bed Model Layout — Channel A

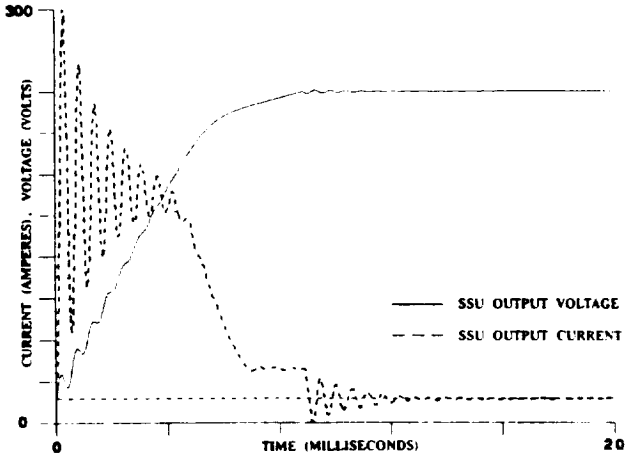

Fig. 7 SSU Model — Start Up Wave Forms

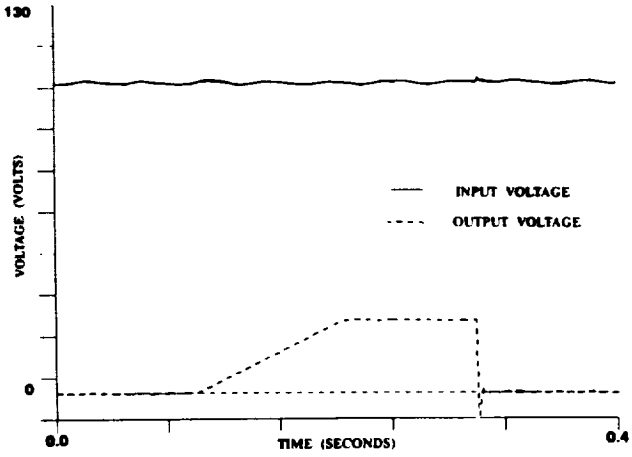

Fig. 8 LCU Model — Start up & Shutdown Voltage Wave Forms

Figures 8 and 9 show the input/output voltage and current wave forms, respectively, for an LCU under start up and shut down conditions. The location of the LCU is shown in figure 6. The LCU is designed to slowly ramp up its output voltage to control or eliminate load starting transients. The wave forms show that the LCU output current is free from load transients. There is a transient in the input current due to charging or discharging of the of the LCU input filter.

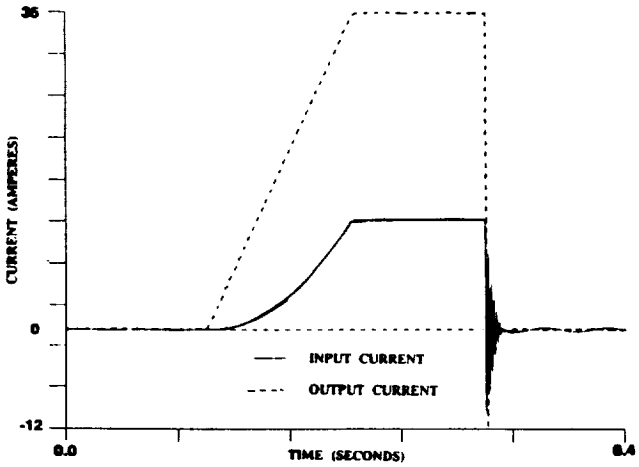

Fig. 9 LCU Model — Start up & Shutdown Current Wave Forms

Case Study No. 2

As described earlier, the function of the test bed protection system is to protect the test bed network as well as individual hardware pieces. Thus, for example, the DDCU is designed to go into a current limit mode when its output is short circuited. The value of the limiting current can be pre-set by the test bed operator.

There are some concerns about DDCUs operating from the same input bus. This test case was selected to investigate those concerns.

A DDCU appears as a constant power load to the bus it is connected to. When another DDCU, connected to the same bus, experiences a load disturbance (or a short circuit) the first DDCU can shift to an undesirable operating condition while keeping the power (load) constant and, therefore, a cause of concern.

The relative isolation of the outputs of two DDCUs connected to the same input bus is of interest. It is desirable that any disturbance at the output of one DDCU should have minimal effect on the output of the other DDCU.

Figures 10 and 11 show the output voltage and current, respectively, of a DDCU subjected to a short circuit (fault) at its output terminals. Upon the application of the fault the output voltage at the faulted DDCU goes to zero and remains at that value for the duration of the fault. The fault current, after an initial transient, is limited to the value preset by the user. Please note that the DDCU recovers and resumes normal operation when the fault is removed. The concerns about DDCUs being connected to the same input bus were not substantiated by this case. First, the unfaulted DDCU appears to behave properly during the application and removal of fault at the output of the other DDCU. Secondly, the output voltage of the unfaulted DDCU shows very little change due to a fault at the output of the other DDCU, as seen in figure 12. Thus, the outputs of the two DDCUs are well isolated for this test case.

FUTURE WORK

Although an end-to-end model for channel A is now available, the modeling process is not yet complete. Basic switchgear models as well as model of the protection system is under implementation. In addition, the model validation process will continue and the corresponding results will be reported.

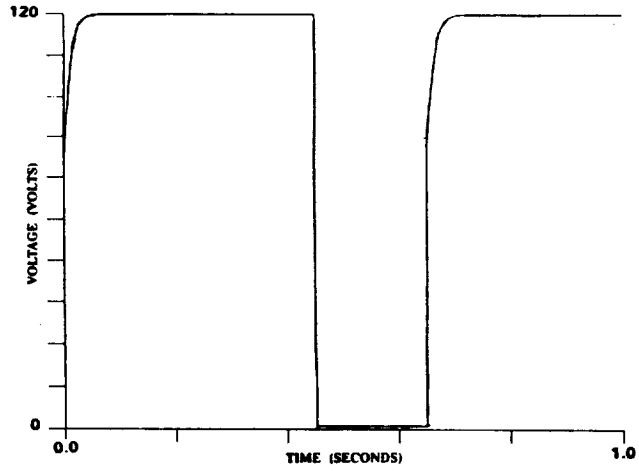

Fig. 10 DDCU Output Voltage — Short Circuit

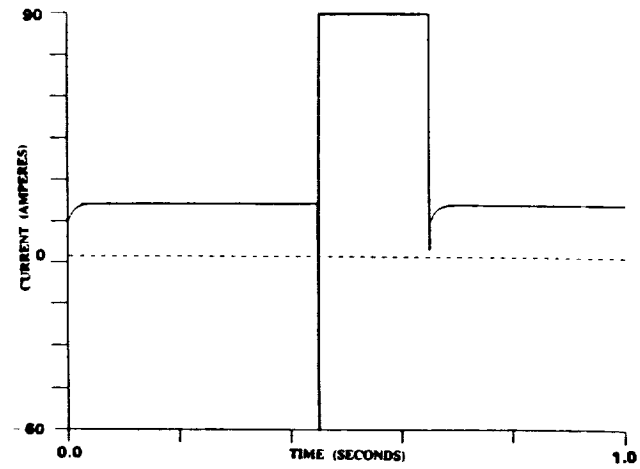

Fig. 11 DDCU Output Current — Short Circuit

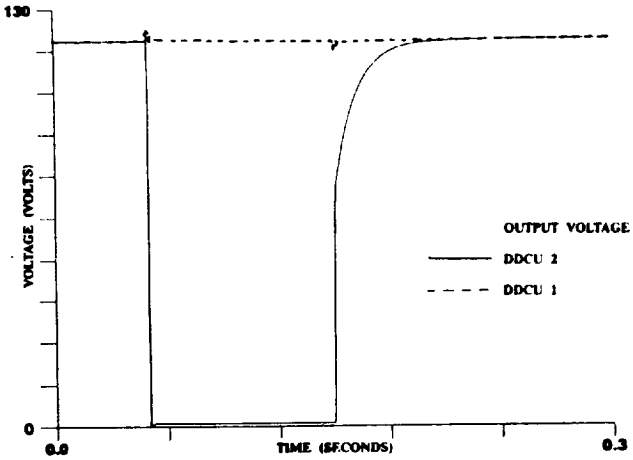

Fig. 12 Faulted & Unfaulted DDCU: Output Voltages

Other future work includes modeling of the Channel B hardware components and the *prime program* control and protection scheme to evaluate its performance in the test bed environment.

CONCLUSIONS

A system level end-to-end computer simulation model of the PMAD DC test bed has been generated using EMTP. Circuit level models were generated for some of the components while functional models were generated for all the components. When using functional component models, the system level model executes fast enough to serve as an adjunct tool for the test bed developer and user. The test bed model is designed on a modular basis for quick reconfiguration between cases. Models are validated against test bed data at various stages. There is good agreement between the simulation results and test data for the purposes of the end-to-end simulation. The test bed team now has a valuable simulation tool to aid in test bed hardware integration, operation, and evaluation.

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The public domain version of EMTP(aka ATP) was utilized to generate the system level model of EPS. Component models resulted from work described in [5,6].

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